Thermal-Aware Address Decoding in Scratchpad Memories

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ABSTRACT

Scratchpad memories (SPMs) have become a promising on-chip storage solution for embedded systems from an energy, performance and predictability perspective. The thermal behavior of these types of memories has not been considered in detail. The thermal behavior in silicon devices plays an important role in the reliability of these systems and static (leakage) power consumption. In this short note, we outline a scheme to reduce the peak temperature and thermal cycling of SPMs in applications that have regular access patterns on their data structures. The key idea of our method is to physically distribute these accesses evenly over the whole memory area.

KEYWORDS: Temperature Aware Design; Scratchpad Memory; Streaming Application; Hot Spot;

1 Motivation

Scratchpad memories (SPMs) have become an efficient replacement for caches in novel embedded systems, due to their lower energy/area cost and better predictability [Ban02]. The drastic increase of the power density of digital circuits by shrinking feature sizes of transistors has become an important concern in VLSI industry. Higher power density translates to a higher local chip temperature. Many multimedia applications that are mapped onto embedded systems have a regular memory access pattern (e.g. motion estimation in an H.263 encoder). In general, SPM allocation techniques place elements on consecutive addresses. So, SPMs with a traditional address layout will have a lot of accesses to a small region of the SPM when running this type of applications. This will incur a higher power density in the highly accessed region which will lead to a moving hotspot over the SPM during the execution of the application and as a result it leads to thermal cycling. This short note outlines a novel SPM address decoding strategy that takes the regular memory access pattern found in streaming applications into account. The proposed address decoder leads to a balancing in the access pattern, power density, and temperature distribution over the physical area.

2 Logical to Physical Address Mapping

Multimedia applications typically process various types of video or audio streams. These streams are placed as a sequence of frames or macro-blocks in the memory system. Appli-

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[2]Supported by the Dutch Technology Foundation STW, project NEST - 10346

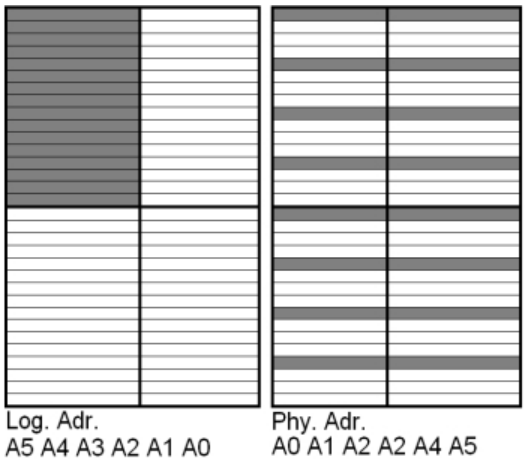

Figure 1: Logical to physical address mapping.

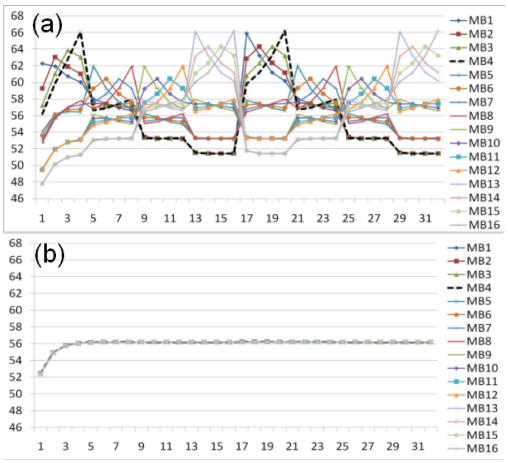

Figure 2: Temperature of memory banks.

cations access this data in a regular manner. During a short time period (e.g. the processing time of one macro-block of an image) one region of the memory (e.g. storing a macro-block) is accessed heavily. As a result of this high activity, the power density of the accessed region increases and the local temperature rises. Because the subsequent memory accesses of an application are typically to subsequent logical addresses, an even distribution of accesses across the SPM can be achieved by maximizing the physical distance between consecutive logical memory addresses. The desired effect can be achieved via address decoding by just mirroring the address bits. By mirroring the logical addresses, consecutive accesses within one bank are distributed over all banks of the SPM. Fig. 1 illustrates our address decoding scheme with a memory that consists of 4 banks and 16 words inside each bank. It shows that our address decoding scheme distributes consecutive logical addresses over the entire SPM. Note that this address mirroring technique requires no extra silicon area or performance loss.

3 Case Study

A case study on a motion estimation algorithm has been performed to evaluate our thermal-aware address decoding technique. This application uses an image window of 4x4 macro blocks that it accesses in a regular pattern. We allocated this image window to an SPM and we performed a thermal simulation of the SPM using HotSpot [Hua06]. Fig. 2.(a) shows the average temperature (°C) of all 16 memory banks (MBs) in an SPM with a traditional address decoder. The temperature distribution obtained with our address decoder is shown in Fig. 2.(b). The results show clearly that our address decoder is able to reduce the thermal cycling significantly (from 14.8°C to 0.1°C). The results also show that our decoder reduces the peak temperature by 10.0°C.

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